Features:

- Supports 9.95Gb/s to 11.3Gb/s bit rates
- Hot-pluggable XFP footprint
- Single LC for Bi-directional Transmission
- Maximum link length of 10km
- Built-in 1270/1330 WDM
- Uncooled 1270nm or 1330nm DFB Laser.
- Low Power dissipation 1.5W(TYP)
- No Reference Clock required
- Built-in digital diagnostic functions
- Temperature range 0°C to 70°C
- Very low EMI and excellent ESD protection
- RoHS Compliant Part

Applications:

- 10GBASE-LR/LW 10G Ethernet
- 1200-SM-LL-L 10G Fibre Channel

Description:

POFLINK's PLX-10G-2733-10& PLX-10G-3327-10 Bi-directional 10Gb/s (XFP) transceivers are compliant with the current XFP Multi-Source Agreement (MSA) Specification. They comply with 10-Gigabit Ethernet 10GBASE-LR/LW per IEEE 802.3ae and 10G Fibre Channel 1200-SM-LL-L. Digital diagnostics functions are available via a 2-wire serial interface, as specified in the XFP MSA.

Specification:

- **Electrical Characteristics (Condition: $T_a=T_{OP}$)**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	Vcc3	3.13		3.45	V	
Supply Current – Vcc3 supply	Icc3		300	500	mA	
Module total power	P		1.5	2	W	
Transmitter						
Input differential impedance	Rin		100		Ω	1
Differential data input swing	Vin,pp	120		820	mV	
Transmit Disable Voltage	VD	2.0		Vcc	V	
Transmit Enable Voltage	VEN	GND		GND+ 0.8	V	
Transmit Disable Assert Time				10	us	

Shenzhen POFLink Communication Equipment Co., Ltd.
4F,Landfeng Building Kefa Rd Hi-Tech Industrial Park, Nanshan, Shenzhen, China
Tel: +86 755 26014656 Fax: +86 755 26532516
E-mail: info@poflink.com Http://www.poflink.com

Receiver						
Differential data output swing	Vout,pp	340	650	850	mV	
Data output rise time	tr			38	ps	2
Data output fall time	tf			38	ps	2
LOS Fault	VLOS fault	Vcc – 0.5		VccHOST	V	3
LOS Normal	VLOS norm	GND		GND+0.5	V	3
Power Supply Rejection	PSR	See Note 4 below				4

1. After internal AC coupling.
2. 20 – 80 %
3. Loss Of Signal is open collector to be pulled up with a 4.7k – 10kohm resistor to 3.15 – 3.6V. Logic 0 indicates normal operation; logic 1 indicates no signal detected.
4. Per Section 2.7.1. in the XFP MSA Specification.

- **Optical Characteristics (Condition: $T_a=T_{OP}$)**

Parameter		Symbol	Min	Typ	Max	Unit	Ref.
Transmitter							
Operating Date Rate		B	9.9		11.3	Gb/s	
Bit Error Rate		BER			10^{-12}		
Maximum Launch Power		P_{MAX}	-8.2	-3	+0.5	dBm	1
Optical Wavelength	PLX-10G-2733-10	λ	1260	1270	1280	nm	
	PLX-10G-3327-10		1320	1330	1340		
Optical Extinction Ratio		ER	3.5			dB	
Sidemode Supression ratio		SSR_{min}	30			dB	
Rise/Fall Time (20%~80%)		T_r/T_f			50	ps	
Average Launch power of OFF Transmitter		P_{OFF}	-30			dBm	
Tx Jitter		T_{xj}	Compliant with each standard requirements				
Optical Eye Mask			IEEE802.3ae				2
Receiver							
Operating Date Rate		B	9.9		11.3	Gb/s	
Receiver Sensitivity		R			-12.6	dBm	2
Maximum Input Power		P_{MAX}	0			dBm	2
Optical Center Wavelength	PLX-10G-2733-10	λc	1320	1330	1340	nm	
	PLX-10G-3327-10		1260	1270	1280		
Receiver Reflectance		Rrx			-12	dB	
LOS De-Assert		LOS_D			-15	dBm	
LOS Assert		LOS_A	-25			dBm	
LOS Hysteresis			1			dB	

Notes:
1. The optical power is launched into SMF.
2. Measured with a PRBS 2^{-31}-1 test pattern @10.3125Gbps BER<10^{-12}.

- **Absolute Maximum Ratings**

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{ST}	-40	+85	℃
Operating Tempature	T_{IP}	0	+70	℃
Supply Voltage	V_{CC3}	-0.5	+4.0	V

- **Recommend Operation Environment:**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	+3.1	3.3	+3.5	V
Operating Temperature	T_{OP}	0	-	+70	℃

Pin Assignment:

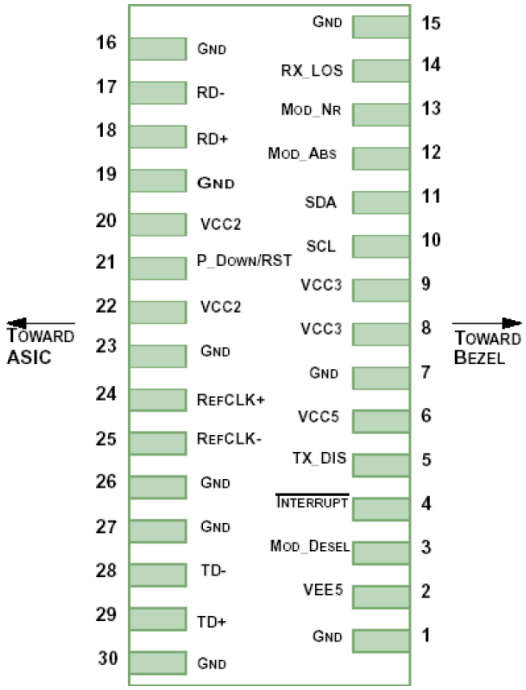


Diagram of Host Board Connector Block Pin Numbers and Name

Pin Description:

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Module Ground	1
2		VEE5	Optional -5.2 Power Supply - Not required	
3	LVTTL-I	Mod-Desel	Module De-select; When held low allows the module to , respond to 2-wire serial interface commands	
4	LVTTL-O	$\overline{\text{Interrupt}}$	Interrupt (bar); Indicates presence of an important condition which can be read over the serial 2-wire	2

			interface	
5	LVTTL-I	TX_DIS	Transmitter Disable; Transmitter laser source turned off	
6		VCC5	+5 Power Supply	
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I	SCL	Serial 2-wire interface clock	2
11	LVTTL-I/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Module Absent; Indicates module is not present. Grounded in the module.	2
13	LVTTL-O	Mod_NR	Module Not Ready;	2
14	LVTTL-O	RX_LOS	Receiver Loss of Signal indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver inverted data output	
18	CML-O	RD+	Receiver non-inverted data output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply – Not required	
21	LVTTL-I	P_Down/RST	Power Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset	
			Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply – Not required	
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock non-inverted input, AC coupled on the host board – Not required	3
25	PECL-I	RefCLK-	Reference Clock inverted input, AC coupled on the host board – Not required	3
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter inverted data input	
29	CML-I	TD+	Transmitter non-inverted data input	
30		GND	Module Ground	1

Note
1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15Vand 3.6V.
3. A Reference Clock input is not required .

Digital Diagnostic Functions:

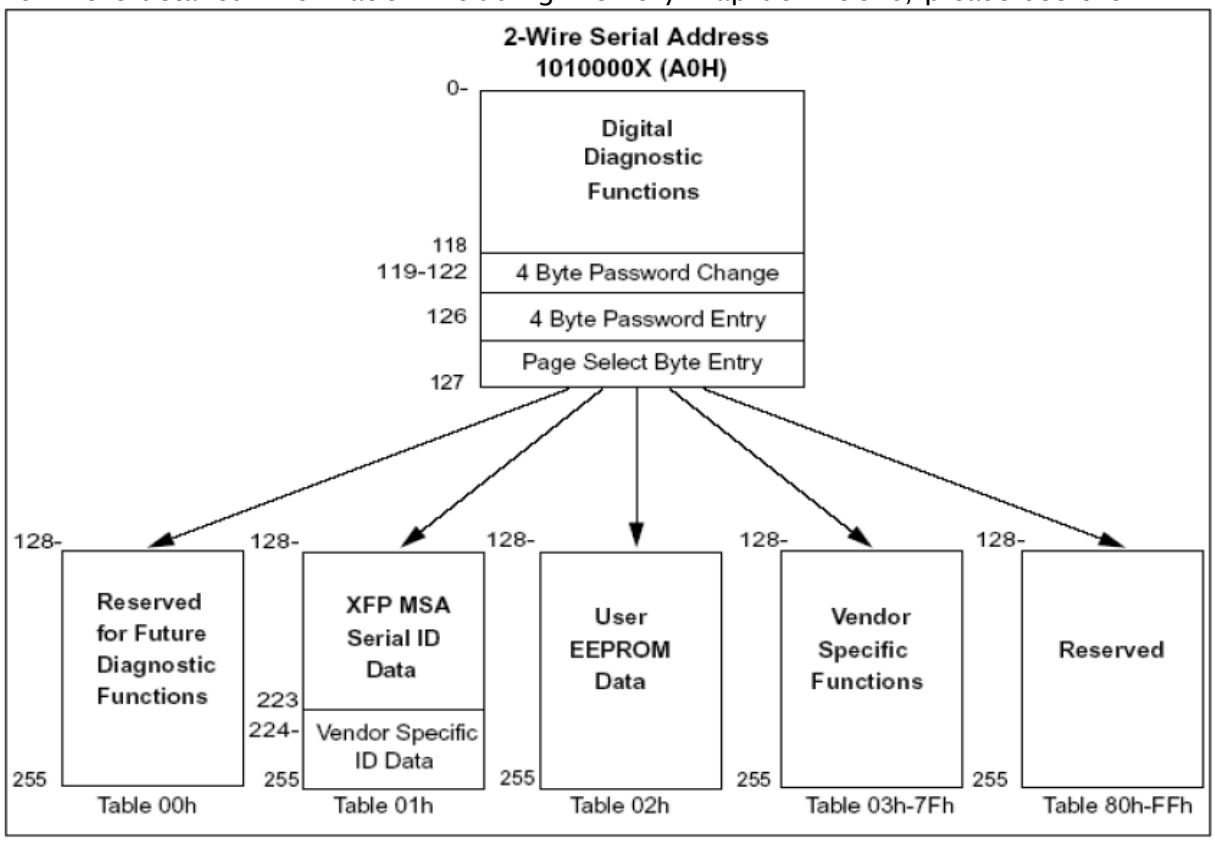
As defined by the XFP MSA 1 , Poflink's XFP transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage

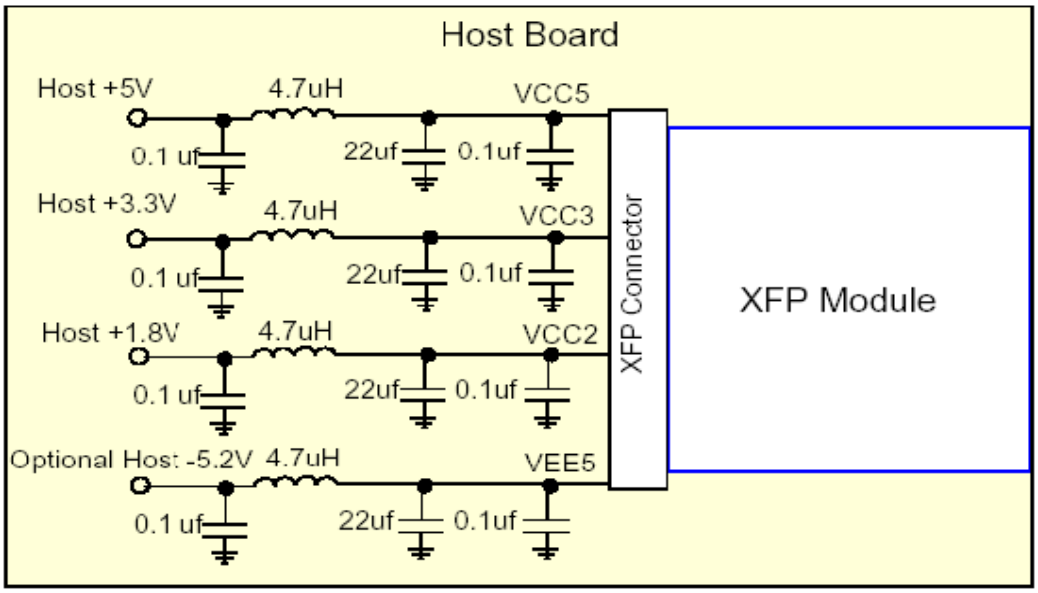
It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.
The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the XFP transceiver into those segments of its memory map that are not write-protected.

The negative edge clocks data from the XFP transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

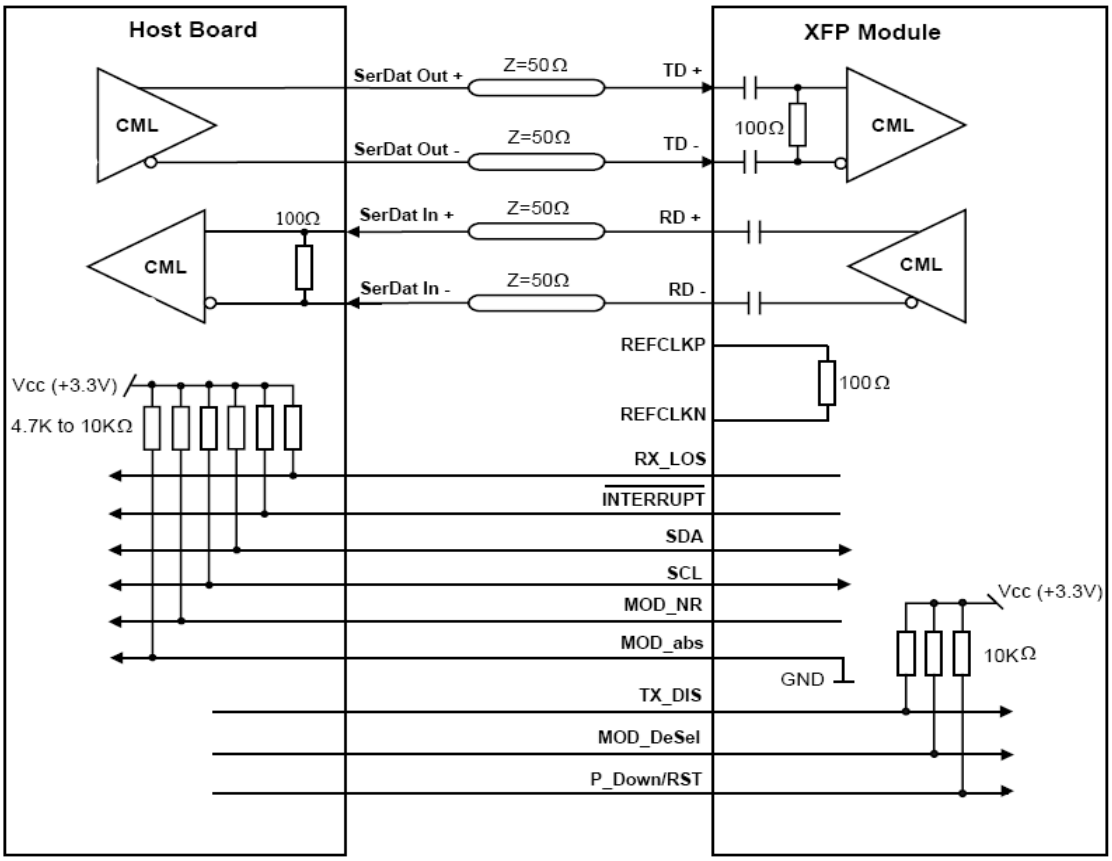
For more detailed information including memory map definitions, please see the XFP MSA Specification.



Recommended Circuit:

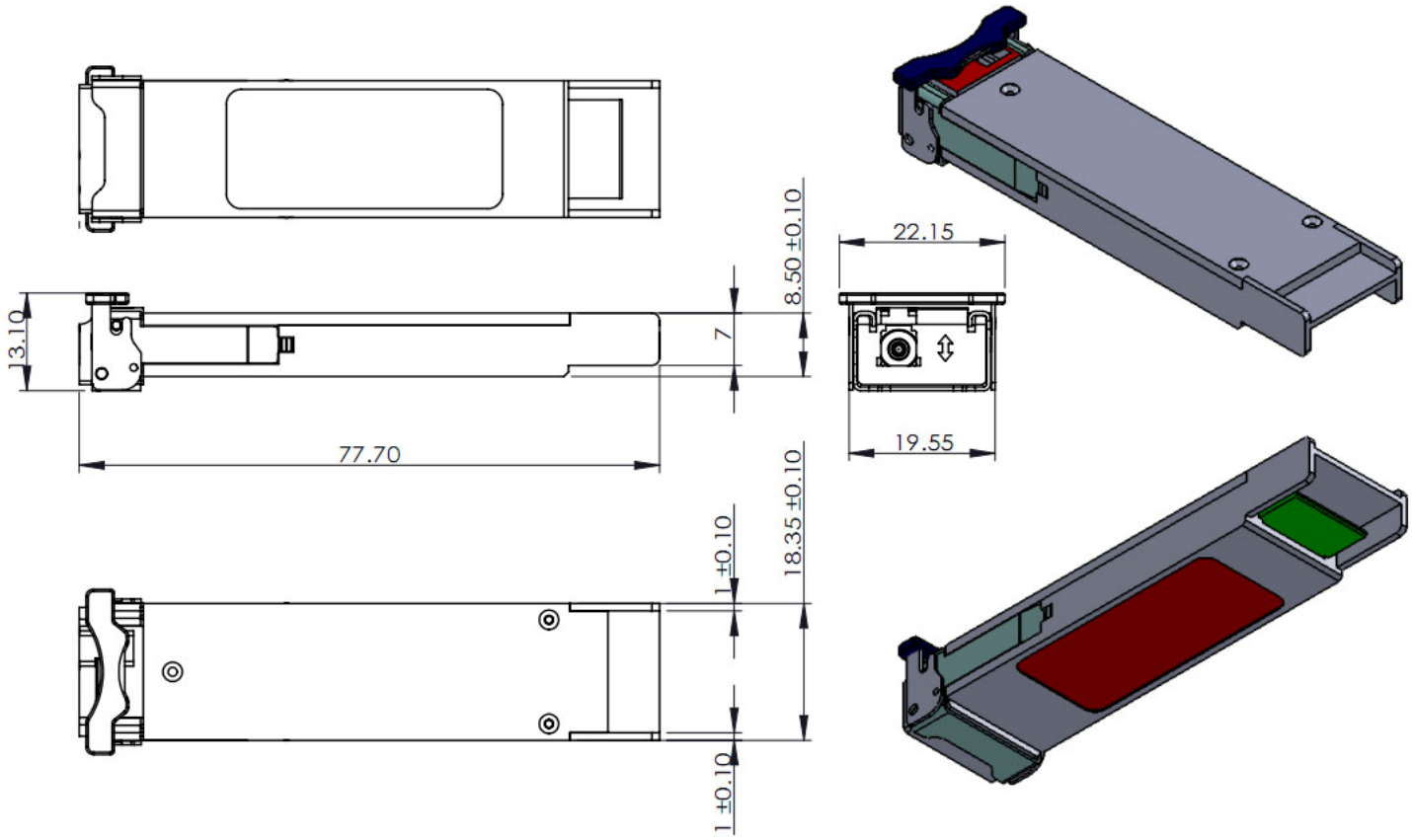


Recommended Host Board Power Supply Circuit



Recommended High-speed Interface Circuit

Mechanical Dimensions:



Shenzhen POFLink Communication Equipment Co., Ltd.
4F,Landfeng Building Kefa Rd Hi-Tech Industrial Park, Nanshan, Shenzhen, China
Tel: +86 755 26014656 Fax: +86 755 26532516
E-mail: info@poflink.com Http://www.poflink.com